NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA, SURATHKAL
राष्ट्रीय प्रौद्योगिकी संस्थान कर्नाटक, सुरत्कल
P.O SRINIVASNAGAR, MANGALORE - 575025

IRIS

EC Call Letter List

M Tech. (Research), 2025 - 26

The following applicants have been selected for written exam and/or interview for the department for the department of Electronics and Communication Engineering for M Tech. (Research) Programme. The applicants are requested to go through additional information provided in their Call letters.

#	Name	Reference Number	Branch/Specialisation
1	K Anusha	MTR2025VL0037	VLSI Design
2	DURGESH	MTR2025VL0041	VLSI Design
3	Asik Babu A	MTR2025CN0006	Communication Engineering and Networks
4	PATNAM PARTHASARATHI	MTR2025VL0043	VLSI Design
5	Supreeth A	MTR2025VL0044	VLSI Design
6	THARUN D GOWDA	MTR2025VL0046	VLSI Design
7	Raman Kumar Jha	MTR2025VL0045	VLSI Design

Head Of Department
Electronics and Communication Engineering

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EC Call Letter List

M Tech. (Research), 2025 - 26

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA SURATHKAL
P.O. SRINIVASNAGAR, MANGALURU-575 025
Telephone: 0824-2473046, Website: www.ece.nitk.ac.in

Date: 21-11-2025

Shortlisted candidates for M Tech (Research / Sponsored) Programme–
Written Aptitude Test / Interview for the year 2025-26 (December Session)

With reference to your application for admission to M Tech (Research / Sponsored) Programme in the department of Electronics and Communication Engineering, you are requested to appear for the Written test/Interview at NITK Surathkal. You should produce all the original records such as Date of Birth Certificate, GATE Score Card, Degree Certificate and Marks Cards of all semesters (UG programme), if result of the final year exam is awaited then provide a certificate from the head of your institution which states that you are the final year student of (branch) appearing / appeared for the final year / semester examination during academic year 2024-25 and results are awaited, SC/ST/OBC/EWS certificate (if applicable as per proforma), OBC / EWS certificate should be obtained from competent authority as specified in the NITK website and must be dated on or after April 1, 2025, Person with disability certificate (if applicable), Sponsorship letter (if applicable), Conduct Certificate and valid photo identity card. Please keep a self-attested photocopy of all these certificates readily available at the time of interview.

Department	Department of Electronics and Communication Engineering
Place of Reporting	Department of Electronics and Communication Engineering, NITK Surathkal
Document verification	December 09, 2025, 9:00AM onwards
Written Test Date and Time	December 09, 2025, 2:00 PM at ECE Department
Announcement of shortlisted candidates for interview	December 09, 2025, 4:00 PM
Interview Date and Time	December 10, 2025, 9:00AM Onwards, Meeting room, ECE Department

NOTE:

1. Candidates should be prepared to appear for a written Aptitude Test before the interview.
2. Fee Structure for M Tech (Sponsored / Research) programme and Course syllabus are provided on Institute's website, i.e. www.nitk.ac.in. A copy of the syllabus for the aptitude test is given in a separate page.
3. Full-time/External Registrants - sponsored from Industry or other organizations, should have been serving in the sponsoring organisation for a period of **at least 2 years** after qualifying degree and have to produce a letter from their employer stating that the candidate is deputed for M Tech / M Tech (Research) in the Institute on full salary during the study period. The employer should indicate that the candidate will not be withdrawn midway before the completion of the course. (Sponsorship letter should be in the format provided in the Application Form).
4. Candidates who have not submitted marks of final examination along with application form shall produce the same at the time of admission if available.
5. Your candidature for this test is provisional & is subject to your fulfilling the educational qualifications & other criteria prescribed for the programme as mentioned in the Information Brochure, failing which your candidature can be summarily rejected after verification/scrutiny at a later stage.
6. Please keep the Admit Card ready during the offline test and interview. You are responsible for safe custody of the Admit Card and in the event of any other person using this Admit Card, the responsibility lies on you to prove that you have not used the service of an impersonator.
7. Please note that no expenses shall be payable for appearing in the written test/Interview.

Sd/ -
Head of the Department

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Date: 21-11-2025

Syllabus for M. Tech. (Research) Aptitude Test- December 2025

Date and time for:

- **Document verifications:** December 09, 2025, 9:00 AM onwards
- **Written Test:** December 09, 2025, 2:00PM to 3:00PM.
- **Interview**: December 10, 2025, 9:00AM onwards

Question Paper format: It is a common paper for all the three streams offered by Department of Electronics and Communication Engineering. There will be 20 questions and all questions are compulsory. The questions are in the MCQ format.
Marking scheme: Every correct answer: 1 mark, Every wrong answer: -0.25 mark.

Note: Total duration of Exam is one hour. Use of Calculator is permitted.

Linear Algebra, Calculus, Differential and Difference equations. Numerical methods, Transforms, Linear circuits and networks, Electronic Components and Devices, Analog Electronics, Digital Electronics, Signals and Systems, Linear and Digital Control Theory.

Electromagnetic Waves, Probability and Random Processes, Communication Theory, Communication Circuits, Transmission Lines, Wave Guides, Antennas, Microwave devices and Circuits, Data Communications, Communication Networks, Satellite Communication, Optical Communication.

Time domain analysis of discrete-time systems - Basic discrete time signals, discrete-time Fourier Series, Z Transform – definition and properties, Discrete-time Fourier Series and its properties, Properties and applications of DTFT. Relationship between time, Z- and frequency domains, DFT fundamentals and Properties of DFT, FIR and IIR filters.

Algorithm analysis, Asymptotic notations. Divide and Conquer algorithms, Analysis of divide and conquer algorithms, sort and search algorithms, Data structures, Linked list, stacks, queues and graphs.

Linear and Digital ICs, Digital System Design, VLSI Technology, CMOS VLSI, Mixed Signal Design, HDL, Data converters, Microprocessors, Computer Architecture and organization, Logic Synthesis, DSP Architectures, Embedded Systems.

Weightage of different academic components for evaluation (As per the information brochure):

MTech (Research) and MTech (Sponsored)

UG (Academic performance in the qualifying examination)	10%
GATE	70%
Written Test	10%
Technical Presentation/ Interview (Research Aptitude/ Technical knowledge/ Subject Knowledge)	10%

Head of the Department